REMARKS

Claims 1-4, 6-17, 19-53, 55, 57-62 and 64-74 are now pending in the application. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the remarks contained herein.

REJECTIONS UNDER 35 U.S.C. §§ 102 AND 103

Claims 49-53, 55, 57-62 and 64-74 are rejected under 35 U.S.C. § 102(b) as being anticipated by Jaggar (U.S. Pat. No. 5,701,493). Claims 1-4, 8-17 and 21-26 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Jaggar (U.S. Pat. No. 5,701,493). These rejections are respectfully traversed.

With respect to claim 1, Jaggar fails to show, teach, or suggest at least that each of the plurality of registers has an address having a length of x bits, each of the processor modes has a length of y bits, and **the encoded address has a length that is less than x + y bits**. Instead, Jaggar appears to disclose that the alleged encoded address has a length that is a sum of the lengths of the address and processor modes.

As shown in an exemplary embodiment in FIG. 5 of the present application, an encoder receives an address having a length of 4 or more (x) bits. Similarly, the encoder receives a corresponding processor mode having a length of 2 or more (y) bits. For example, as shown in FIG. 3 of the present application, a register file 206 may receive 5 or more processor modes using 4 or more inputs. The encoder generates an encoded address based on the address bits and the processor mode bits. For example, as shown in FIG. 5, the encoded address has a length of 5 bits. As such, the encoder actually *encodes* (i.e. transfers the data from one format to another) the address and

the processor mode, rather than merely adding the processor mode bits to the end of the address bits. Consequently, the encoded address has a length that is less than x + y bits.

In contrast, Jaggar appears to be absent of any teaching or suggestion that the alleged encoded address has a length that is less than x + y bits. Instead, Jaggar appears to disclose that the encoded address is simply an addition of the processor mode bits to the end of the address bits. Applicants respectfully note that the Examiner fails to provide any support for the allegation that Jaggar discloses this limitation, and merely conclusorily states that the encoded address "has a length...that is less than x + y bits (i.e. less than 4+5=9 bits)(e.g. see Fig. 8)."

Applicants respectfully submit that FIG. 9 of Jaggar fails to disclose that the encoded address has a length that is less than 9 bits. Instead, Jaggar discloses that an address decoder 17 receives the 4 address mode bits **and** the 5 processor mode bits. More specifically,

> a physical register address identifying a particular one of the user mode registers and the exception mode registers is derived from **a combination of the mode bits from the CPSR and an instruction register address as decoded by the register address decoder 17**. (See Column 4, Lines 8-12; Emphasis added).

In other words, Jaggar discloses that the decoder 17 receives a **combination** of the address and mode bits. Neither this portion nor any other portion of Jaggar appears to disclose that the alleged "encoded" address has a length that is less than a mere summation of the address bits and the mode bits.

In view of the foregoing, Applicants respectfully submit that Jaggar fails to show, teach, or suggest at least that the encoded address has a length that is less than x + y

bits. As such, claim 1, as well as its dependent claims, should be allowable for at least the above reasons. The remaining independent claims, as well as their corresponding dependent claims, should be allowable for at least similar reasons.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

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